UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETLIST, INC.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., AND MICRON TECHNOLOGY TEXAS LLC,

Defendants.

Civil Action No. 1:22-CV-00134-LY
Civil Action No. 1:22-CV-00136-LY

JURY TRIAL DEMANDED

DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF

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Defendants ("Micron") hereby provide their reply claim construction brief.

I. VOLATILE / NON-VOLATILE MEMORY SUBSYSTEMS ('833 PATENT, CL 15)

The issue is whether the terms should be construed as a series of volatile/non-volatile memory devices as Micron proposes or expanded to broadly encompass other components present in a memory system (*e.g.*, a controller) as Netlist proposes. Micron's proposal reflects how a person of skill ("POSITA") would have understood the terms. Netlist's proposal expands the terms beyond any cognizable limits and conflicts with its prior *inter partes* review ("IPR") arguments.

There is no dispute that a "subsystem" is part of a larger system. The relevant question is whether the disputed terms should be construed to encompass other memory system components. The answer is no. The claims recite the volatile/non-volatile memory systems separately from at least the "controller" structure. *See* '833 patent claim 16 (reciting "controller"). The specification refers to memory subsystems as distinct from other memory system components. *See, e.g.,* Opening Br., 5 (Figure 1 annotated showing separate memory devices, switches, controller, etc.). During IPR, Netlist argued that the claimed memory subsystems are distinct from other memory system components. *See* Opening Br., Ex. 17 at 16 ("As Patent Owner points out, Petitioner does not explain sufficiently why the controller is a part of the volatile memory subsystem.").

Netlist's argument that a POSITA would understand a memory subsystem can "include other components or elements such as registers, data interconnects and/or control elements" is misleading. Response Br., 2. Memory devices can be built with registers included therein—and Micron's proposal doesn't exclude registered memory devices. In contrast, the parties are disputing whether the terms should be interpretated broadly to encompass "control elements" (*e.g.*, the memory system's controller). As Netlist argued in IPR, they should not.

Indeed, Netlist's attempt to construe the terms to include "interconnects" proves that its interpretation is overly expansive. It defies common sense to consider the lines/buses that connect

memory subsystems to something else (for example to switches) as part of the memory subsystem—they are just as much a part of the "something else" that is being connected. Netlist makes the "interconnect" argument to broaden the disputed terms to encompass unrelated components in a memory system. That interpretation is unsupported and unplausible. Nor do any of Netlist's citations to the specification (Response Br., 2) support its position—those sections merely refer to connecting/coupling components with interconnects & buses and never define the interconnects as part of a volatile/non-volatile memory subsystem.

II. "CONTROLLER" ('833 PATENT, CL 16)

As a primary issue, Netlist relies on questionable authority for this term. Netlist cites *Linear Tech. Corp. v. Impala Linear Corp* for proposition that 112(6) does not presumptively apply "when the structure-connoting term 'circuit' is coupled with a description of the circuit's operation." Response Br., 4-5 (citing 379 F.3d 1311, 1320 (Fed. Cir. 2004)). The Federal Circuit, however, has cautioned against relying on pre-*Williamson* precedent ***and specifically distinguished Linear***. *Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367, 1374 (Fed. Cir. 2020).

Nor is the relied upon *Linear* statement applicable here. First, the term at issue in *Linear* was "circuit," not "controller," and Netlist has not shown how that statement regarding "circuit" is applicable to the "controller" term here. Second, *Linear* relies upon *Apex Inc. v. Raritan Computer, Inc.*, for this statement, but *Apex* explicitly stated that it is not "hold[ing] that the term 'circuit' by itself always connotes sufficient structure" and analyzed whether there was also an identifier claim term that connotes structure, such as an "interface circuit". *See Linear*, 379 F.3d at 1320 (*citing Apex*); *Apex*, 325 F.3d 1364, 1373 (Fed. Cir. 2003). In contrast, because there is no identifier term recited here, "controller" is recited as a stand-alone term, devoid of structure.

Applying post-*Williamson* authority, "controller" is a nonce term that does not provide structure for the claimed functions. For example, this Court has held that "[t]erms such as

'controller' often connote insufficient structure to take the limitation outside the bounds of Section 112(f)." *Incom Corp. v. Radiant RFID, LLC*, No. 1-17-CV-009-LY, 2018 WL 4690934, at *5 (W.D. Tex. Sep. 28, 2018). Such is the case here. Indeed, the present "controller term" is even more bare-bones and structureless than the actual "***tag orientation*** controller" term at issue in *Incom*. *See id.* ("the term "tag orientation controller" fails to recite sufficiently definite structure"). Here "controller" is recited without any limiting identifiers.

Netlist's citations to the intrinsic record fail to "take the [controller] limitation outside the bounds of Section" 35 U.S.C § 112(6). *Id.* Specifically, Netlist only cites language from the specification and claims that merely present functional language or provide non-limiting examples of "potential configurations, such as an FPGA." *See* Response Br., 5-6. Such functionality and non-limiting examples do not connote structure to the term. *See MTD Prods. Inc. v. Iancu*, 933 F.3d 1336, 1343 (Fed. Cir. 2019) (explaining that claim language reciting what a nonce term is "configured to" do is functional); *Microsoft Corp. v. Motorola Inc.*, No. C10–1823JLR, 2013 WL 454268, at *7 (W.D. Wash. Feb. 7, 2013) (finding disclosure of FPGA not sufficient structure) (citing *In re Aoyama*, 656 F.3d 1293, 1299 (Fed. Cir. 2011) for similar proposition).

Nor is Netlist correct in arguing that Micron's proposal is improperly limited to a single embodiment. The '833 patent consistently describes the controller as "separate from the volatile and non-volatile memory subsystems." Opening Br., Ex. 15 at 12; *see also* '833 patent at Abstract, 3:62-64, 4:57-61, 6:54-7:36, 7:66-8:56, 10:19-22, 13:57-14:47, 15:59-16:37, 18:29-20:61. Further, as reflected in Micron's proposed structure, the only disclosure for the claimed functionality is at '833 patent, 6:63-7:40.

Netlist argues that a controller is considered part of the volatile / non-volatile memory subsystems. *See* Response Br., 7 (the specification "never teaches that the controller must be

separate and distinct from the non-volatile memory"). This attempt should be rejected as contrary to the intrinsic record and Netlist's own IPR arguments. *See supra*, Section I.

III. "MODULE CONTROL DEVICE" ('035 AND '608 PATENTS, CL 1)

Like the "control module" in *Williamson*, the "module control device" terms here are governed by § 112(6). *Williamson v. Citrix Online*, *LLC*, 792 F.3d 1339, 1350 (Fed. Cir. 2015). These generic terms provide no structure for the claimed functions. *See* Opening Br., 9-12. The claim emphasizes the black-box nature of these terms because it only recites where the "module control device" is mounted and its function: "(1) receive certain signals for a particular operation from the memory controller via specified signal lines; and (2) output specific signals in response." *See* Response Br., 8; Smith Dec. ¶¶ 34-36.

Netlist's arguments against application of § 112(6) treatment are meritless. *First*, Netlist relies on outdated case law that the Federal Circuit cautions against. *See Egenera*, 972 F.3d at 1374. Further, Netlist relies on *Abacus*, which based its decision on *Lighting World*'s heightened burden that was overruled in *Williamson*. *Mass. Inst. of Tech. v. Abacus Software*, 462 F.3d 1344, 1356 (Fed. Cir. 2006); *Williamson*, 792 F.3d at 1349 (concluding heightened bar in *Lighting World* is unjustified). Accordingly, Netlist's cited opinions are inapposite.

Second, Netlist's arguments about the purported structure required by the claims are demonstrably false. Netlist's urged structure involves only the input (*i.e.*, "(1) connections to signal traces for receiving commands from a memory controller") and output (*i.e.*, "(2) connections to command signal traces that couple to the module control device and other components on the memory module"), but provide no detail as to how a module control device is implemented. Response Br., 8. Nor can a recognition of how the module interacts with other components provide structure here. Indeed, Netlist's argument that the claimed module would include unspecified "internal functional units" (Response Br., 8) emphasizes how the patent lacks

any description of its internal structure. *Id*. Where, as here, the structure for a § 112(6) claim limitation is guess-work, the claim should be held invalid as indefinite.

Third, Netlist's arguments about the context of the claim are meritless. Response Br., 8-9. Even if "module" was rewritten as "memory module," as Netlist seems to urge (*id.*, 10), the re-written term "a memory module control device" would only provide detail as to what was being controlled—not the claimed module doing the controlling. *Egenera*, 972 F.3d at 1374 ("Mere inclusion of a limitation within a structure" is not enough.) Consequently, the claims' context provides no insight into the structure of the claimed "module control device."

Fourth., Netlist cannot salvage its position by pointing to passages in the specification for structure. *MTD Prods.*, 933 F.3d at 1344 (explaining that a structure disclosed by the specification "does not necessarily mean that the claim term is understood by persons of ordinary skill in the art to connote a specific structure or a class of structures"). Netlist cites two passages that explain how the inputs of the "module control device" are coupled to lines and its location—but neither passage describes any internal structure. *See* Response Br., 10-11 (citing '035 patent at 4:25-33; '608 patent at 4:27-35). The remaining cited passages are unrelated to the claimed functions, *see id.* at 11 (citing '035 patent at 8:9-12, 9:49-54; '608 patent at 9:52-57). Accordingly, the specifications do not provide a description of the internal structure of a "module control device."

Micron's opening brief explained that these "module control device" limitations are indefinite for lack of corresponding structure for performing the recited functions. *See* Opening Br., 13. Notably, Netlist does not (and cannot) identify even one structure that is clearly linked to performing the claimed functions. *Default Proof Credit Card Sys. v. Home Depot U.S.A.*, Inc., 412 F.3d 1291, 1298 (Fed. Cir. 2005). Netlist's cited passages merely present functional language

without any clearly linked structure for the claimed functions. *See, e.g.*, '035 patent at 4:25-33, 4:63-5:8, 5:55-63; '608 patent at 4:27-35, 4:65-5:10, 5:58-66.

IV. "LOGIC" ('035 PATENT, CL 1)

The claimed "logic" is no more than a "'black box recitation of structure' that is simply a generic substitute for 'means.'" *Egenera*, 972 F.3d at 1375. The remaining claim language emphasizes the black-box recitation of structure by specifying only the claimed logic's functions (*i.e.*, "responding to the module control signals", "enabling the data paths" and "obtain timing information. . . ." and "control timing of the respective data. . . .")—none of which provides insight into the logic's structure. *MTD Prods.*, 933 F.3d at 1343. Without any insight into its internal structure, the term fails to provide a POSITA with "sufficient structure for performing" its claimed functions rendering it a means-plus-function limitation. *Williamson*, 792 F.3d at 1349.

Netlist's arguments to the contrary are meritless. *First*, Netlist's arguments rely on pre-*Williamson* opinions that the Federal Circuit cautions against using. *Egenera*, 972 F.3d at 1374. Netlist's other cases rely on the same outdated authority making them inapposite.

Second, Netlist's attempts to distinguish this case from *Egenera* are meritless. In doing so, Netlist argues that the that the term "logic" ***must*** "refer to circuity" in the context of the claimed memory modules. Response Br., 16. But the '035 patent's specification refers to "logic circuit," which would make "logic" superfluous if it means "circuit." *See* '035 patent, 13:44-48 (referring to "a logic circuit (*e.g.*, a majority decision circuit)"), 14:60-65. Indeed, Netlist contradicts itself on this issue: for one of its other patents, Netlist listed a variety of potential "logic" elements not limited to mere circuitry. Response Br., 23 ("[T]he claimed 'logic' elements can be. . . . 'a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, [or] a complex programmable-logic device (CPLD).'"). These possibilities demonstrate that the claimed "logic"

has no specific structure. Accordingly, the term "logic" is "so broad and formless as to be a generic black box." *Egenera*, 972 F.3d at 1374. Nor is this a case like in *Sonrai Memory Ltd. v. Oracle Corp.*, No. 1:22-CV-94-LY, 2022 WL 800730, at *10 (W.D. Tex. Mar. 16, 2022), where the court found the "logic" had a corresponding structure of "memory controller," which the parties agreed on construction "indicat[es] the term connotes sufficient structural meaning." Indeed, even if "logic" includes circuity, that alone does not provide "sufficient" structure because the remaining claim language "says nothing about the structure of the circuit." *Limestone Memory Sys. LLC v. Micron Tech., Inc.*, No. 2:12-cv-1369, 2019 WL 6655273, at *19 (C.D. Cal. Sep. 11, 2019); *see Egenera*, 972 F.3d at 1374 ("the question is not whether 'logic' is utterly devoid of structure but whether the claim term recites sufficient structure to perform the claimed functions").

Third, Netlist argues that because the buffer circuit includes the claimed "logic" and interacts with other components, "logic" designates structure. Not so. Although "logic" may be located inside a buffer circuit, that does not "automatically render the limitation itself sufficiently structural." *Egenera*, 972 F.3d at 1374. Likewise, the interactions between "logic" and other memory components provide little to no insight as to the structural makeup of "logic." Smith Decl., ¶ 41. *Finally*, Netlist's argument about how the specification describes the structure for "logic" cannot salvage its argument. *MTD Prods.*, 933 F.3d at 1344.

Micron's opening brief explained that this limitation is indefinite for lack of corresponding structure for performing the claimed functions of "logic." *See* Opening Br., 15–16. In response, Netlist does not (and cannot) identify even one structure that qualifies as the corresponding structure. At most, Netlist's cited passages repeat a claimed function without clearly linking that function to any structure. *See, e.g.*, '035 patent at 10:47-66, 12:7–22, 14:52-17:49, 18:9-15, and 18:63-19:7. To the extent that Netlist identifies isolation device 118 or command processing

circuit 640 as the "corresponding" structure for "logic," the specification treats both as a black box without any explanation of its internal structure. *See generally* '035 patent.

V. "COMMAND PROCESSING CIRCUIT" ('608 PATENT, CL 1)

The "command processing circuit" limitation is a means-plus-function limitation because it recites a generic term without structure to perform certain functions. *See* Opening Br., 16-18. The surrounding claim language emphasizes the "black-box recitation of structure" by specifying only functions (*i.e.*, "(1) receive and decode module control signal"; "(2) control the data path. . . . ; (3) control at least one tristate buffer; and (4) determine an amount of delay for a data signal. . . . "). Response Br., 17; *Williamson*, 792 F.3d at 1350; Smith Dec. ¶¶ 47-48. And the prefix "command processing" does not impart any structure to the term "circuit," which the '608 patent uses in its general sense. Smith Decl., ¶ 47. In doing so, the claimed "command processing circuit" does not recite "sufficient structure for performing that function," thereby making it a means-plus-function limitation. *Williamson*, 792 F.3d at 1349; *Limestone*, 2019 WL 6655273, at *17-19.

Netlist's arguments to the contrary are meritless for at least three reasons. *First*, Netlist's arguments again rely on pre-*Williamson* law. *See* Response Br., 16-17 n.6; *Egenera*, 972 F.3d at 1374. Netlist's other cases rely on the same outdated authority making them inapposite.

Second, Netlist argues that a POSITA would understand from the surrounding claim language that the "command processing circuit" would include components, such as a receiver circuit and command signal driver. But the claimed functions, like those in *Limestone*, "say nothing about the structure of the circuit." *Limestone*, 2019 WL 6655273, at *19; Smith Dec. ¶ 48. Netlist's explanation fails to address what internal components would perform the remaining claimed functions: "control[ling] a data path" or determine "an amount of delay for a data signal. . . ." '608 patent, 19:47, 19:53-54. Without doing so, Netlist's argument fails to explain how the "command processing circuit" has sufficient definite structure to perform every claimed function. *Williamson*,

792 F.3d at 1351-52. *Third*, Netlist's argument about how the specification describes the structure for "command processing circuit" cannot salvage its argument that the disputed term is not a means-plus-function. *MTD Prods.*, 933 F.3d at 1344.

Micron's opening brief explained this limitation is indefinite because it lacks a corresponding structure for performing the claimed functions of a "command processing circuit." *See* Opening Br., 19. In response, Netlist does not (and cannot) identify even one structure that qualifies as corresponding structure. *Default Proof*, 412 F.3d at 1298; Response Br., 19-20. Netlist's cited passages, at most, repeat the claimed function without clearly linking that function to any structure. *See, e.g.*, '608 patent at 10:50-11:2, 12:11-26, 14:57-17:54, 18:14-20, and 19:1-12. To the extent that Netlist identifies command processing circuit 640 as the "corresponding" structure, the specification provides no explanation of its internal structure. *See generally* '608 patent. Even if Netlist's citations include structure performing the claimed function(s), Netlist's passages fail to address what structure "control[s] a data path" or "determine[s] an amount of delay for a data signal. . . ." *Default Proof*, 412 F.3d at 1298; *Williamson*, 792 F.3d at 1351-52.

VI. "BURST OF DATA STROBES" ('314 PATENT, CLS 1, 15, 25, 28)

This term is indefinite because it is susceptible to multiple different interpretations. Netlist provides only a single citation to support its contention that a plain and ordinary meaning for the term "burst of data strobes" can be derived from the intrinsic record. *See* Response Br., 21 (citing the '314 patent at 13:18-22).[1] And to support its alternative construction, Netlist merely provides a self-serving interpretation of Figure 6A of the '314 patent's specification. *See* Response Br., 21.

[1] The remaining citations to the intrinsic record relate generally to data strobe signal (DQS) lines (not "bursts of data strobes") and to the term "burst of N-bit wide data signals," another term that is recited in the '314 patent's asserted claims and that has a meaning that is not disputed by the parties.

However, neither that single citation, nor the Figure 6A discussion, explains what is meant by the claim term "burst of data strobes." In particular, Micron does not dispute that bursts of data strobes can be found in the figures of the '314 patent. Indeed, Micron identified at least two specific meanings, and Netlist identified another.[2] *See* Response Br., 20-21. That, however, is the precise problem – the term is indefinite for being subject to multiple different interpretations. *See* Opening Br., 21 (describing the material distinction between at least the two meanings identified by Micron from the specification and the indefiniteness implications of the materially different meanings).

Netlist's argument that *Dow* and *Teva* are inapplicable here is meritless. Neither case hinged on differences in precise mathematical calculations, as suggested by Netlist. In *Dow*, "[t]he question [was] whether the existence of multiple methods leading to different results without guidance in the patent or the prosecution history as to which method should be used renders the claims indefinite." *Dow Chem. Co. v. Nova Chems. Corp.*, 803 F.3d 620, 634 (Fed. Cir. 2015). In *Teva*, the issue was "that 'molecular weight' or average molecular weight can be ascertained by any of three possible measures: Mp, Mn, and Mw. [But] [t]he claims do not indicate which measure to use." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1344 (Fed. Cir. 2015). Thus, the indefiniteness issues in *Dow* and *Teva* are similar to the indefiniteness issue here—whether the claims, in light of the intrinsic record, fail to inform, with reasonable certainty, a POSITA which of the multiple different meanings of the term "burst of data strobes" is applied in the claims. As described above and in Micron's opening brief, the claims fail to provide the requisite clarity. As a result, all the claims that use the term "burst of data strobes" are indefinite just like the claims in *Dow* and *Teva* were found indefinite.

[2] At best, all the alternative construction does is add another possible meaning to the mix of multiple meanings.

VII. "LOGIC" ('314 PATENT, CLS, 1, 15, 25)

Netlist's reliance on *Rodime PLC v. Seagate Tech., Inc.*, 174 F.3d 1294, 1303-04 (Fed. Cir. 1999) to assert that the language "coupled to" causes the "logic" term to "denote[] a physical structure" is misplaced. *Rodime* determined that the disputed term (*i.e.*, "said positioning means") included definite structural features, such as "support arms," "a pivot shaft," "a bearing assembly," and "a stepper motor." *Id.*, at 1303. Thus, the *Rodime* claim recited significantly more than the what the "logic" is "coupled to" here. And that the black-box "logic" is "coupled to" something purportedly structural does not make it a "sufficiently" definite structure. *Egenera*, 972 F.3d at 1374 ("the question is not whether 'logic' is utterly devoid of structure but whether the claim term recites sufficient structure to perform the claimed functions."). At most, this language shows the claimed "logic" is connected to another component, which is not enough. *Id.*

Netlist's citations to the specification and to other functionality of the logic recited in the asserted claims also do not take the overall "logic" claim limitations out of the ambit of § 112(6). First, Netlist cites to the specification to show merely that "the claimed 'logic' elements can be selected from a group of physical components" and that there are purportedly "numerous other examples where logic is described as a physical, structural element." Response Br., 23-24. That is not enough—"[t]he standard is whether the ***words of the claim*** [not the specification] are understood by [a POSITA] to have a sufficiently definite meaning as the name for structure." *Williamson*, 792 F.3d at 1349 (emphasis added). The analysis of what should be the specific corresponding structure from the specification for the means-plus-function "logic" limitation is part of the second inquiry regarding the construction of that means-plus-function limitation after it is determined that § 112(6) applies, not the initial inquiry as to whether § 112(6) even applies. *See Egenera*, 972 F.3d at 1372-75; *see also Williamson*, 792 F.3d at 1347-54. Thus, all that the citations to the specification show is that the "logic" can be implemented in various ways. But the

Federal Circuit has already considered the implications of such broad disclosure in a specification and has still held that a "logic" limitation associated with such disclosure is still subject to § 112(6) claim construction. *Egenera*, 972 F.3d at 1374 (considering the district court's explanation regarding the specification's disclosure of how the "logic" is implemented).

Second, Netlist cites to ***other*** claimed functionality of the logic—namely, receiving …, decoding …, generating …, and communicating …—to assert that "the logic must be a specific type of device capable of" performing those ***other*** functions. Response Br., 24-25. However, that does nothing to show that the logic limitations in dispute here recite sufficient structure for performing the claimed functionality at issue here, *i.e.*, the specific "logic" functionality Micron asserts has no corresponding structure. The Federal Circuit has expressly stated that "[w]here there are multiple claimed functions, as we have here, the patentee must disclose adequate corresponding structure to perform all of the claimed functions." *Williamson*, 792 F.3d at 1351-52. Thus, Netlist's arguments relating to ***other*** claimed functionality of the logic are irrelevant to the specific inquiry here regarding the specific "logic" functionality Micron asserts has no corresponding structure.

Turning to the corresponding structure or algorithm for the means-plus-function "logic" limitations at issue here, the '314 patent's specification fails to describe any structure corresponding to the relevant claimed functionality of the means-plus-function "logic" limitations. Stone Decl., ¶ 49. Netlist does not indicate otherwise. Netlist merely identifies numerous places where logic is ***generally described*** in the '314 patent's specification. *See* Response Br., 25. However, nowhere in the disclosure of the '314 patent cited by Netlist, or anywhere else, is there ***any disclosure of any structure that performs the specific claimed "logic" functionality***. Stone Decl., ¶ 49. Indeed, Netlist's string citation falls far short of showing a clear link or association between a structure in the '314 patent's specification and the "logic" functionality at issue here.

VIII. "OVERALL CAS LATENCY . . ." / "ACTUAL OPERATIONAL CAS LATENCY" ('314 PATENT, CLS 1, 15, 25, 28)

There are two disputes for these terms. The first is whether there is a plain and ordinary meaning. Netlist has failed to show that there is a plain and ordinary meaning for these terms.

The second dispute is whether Micron's proposal or Netlist's alternative proposal more accurately reflects the meaning of these terms to a POSITA. As explained in Micron's opening brief, the Court should adopt Micron's proposal because CAS latency was equated with read latency at the time of the invention. *See* Opening Br., 26.

Netlist's response does not compel a different interpretation. For example, Netlist cites various aspects of the claims and specification to argue that the invention allows for read and write commands. Response Br., 26. That fact, however, is not disputed. Memory devices have allowed for read and write commands well in advance of the Netlist patents. Micron's construction does not exclude write commands, it just sets forth how a POSITA would understand the term as a parameter of a memory system that performs read and write commands.

The primary issue with Netlist's alternative proposal and interpreting the terms to refer to both read and write commands, is that it completely removes the concept of latency. For example, for the "overall CAS latency of the memory module" term, Netlist proposes "the delay between: (1) the time when a command is sampled on the memory module, and (2) a time when the first piece of data is available at the data pins of the memory module." *Id* at 25. Netlist ignores, however, that a write command sends the data to be written (with the write command) to the memory module data pins and therefore has "the first piece of data [] available at the data pins of the memory module" ***at the exact same time*** it is "sampled", *i.e.*, when the data to be written is first sent to the memory module with a write command. Similarly, for the "actual operational CAS latency of each of the memory [devices/circuits]" term, Netlist proposes "the delay between: (1) the time

when a command is executed by each of the memory [devices/circuits] . . . and (2) a time when the first piece of data is available at the data pins of each of the memory [devices/circuits]." *Id* at 25-26. Netlist again ignores that a write command is executed by the memory circuits ***at the exact same time*** that the "data [to be written] is available at the data pins of each of the memory [devices/circuits]." *Id.* Netlist's alternative proposal reads latency right out of the claim terms and should be rejected.

IX. "CIRCUITRY . . . CONFIGURED TO . . ." ('314 PATENT, CLS 1, 15, 25, 28)

Netlist relies on claim language reciting how the "circuitry" is "coupled" and what the "circuitry" is "configured to" do to assert that "the claims treat 'circuitry' as a structural limitation." Response Br., 29. But that claim language does not impart sufficiently definite structure into the term "circuitry," and therefore does not disqualify the claim from § 112(6) treatment. *See Williamson*, 792 F.3d at 1351. Here, like *MTD Products*, the claim language recites purely functional language by describing what the "circuitry" is "configured to" despite reciting how the "circuitry" is "coupled" to other components. *MTD Prods.*, 933 F.3d at 1343 ("[w]hile the claim language reciting that the mechanical control assembly is 'coupled to the left and right drive units' connotes structure, the claim language reciting what the mechanical control assembly is 'configured to' do is functional"). In doing so, "the claim format tends to favor [the] position that § 112, ¶ 6 applies." *Id.*; *see also Williamson*, 792 F.3d at 1351. Netlist's reliance on *Inventio*, *Abacus*, *Linear*, *Apex*, and *Rodime* does not dictate a different result because those cases are inapposite for the reasons set forth above. *See* Sections II-V and VII.

Netlist's citations to the specification cannot salvage its argument by identifying structure in the specification. *MTD Prods.*, 933 F.3d at 1344; *Williamson*, 792 F.3d at 1349 ("[t]he standard is whether the words of the claim [not the specification] are understood by [a POSITA] to have a sufficiently definite meaning as the name for structure."); *see* above Section III. Rather than focus

on the *Williamson* standard, Netlist focuses on the ***words of the specification*** and argues that "the '314 Patent [specification] provides sufficient structure for 'circuitry' for performing the claimed functions." *See* Response Br., 29-30.

The '314 patent's specification fails to describe any corresponding structure for the relevant claimed functionality of the means-plus-function "circuitry" limitations, *i.e.*, the "circuitry" functionality Micron asserts has no corresponding structure. Stone Decl., ¶ 59. Netlist does not indicate otherwise. Netlist merely identifies numerous places where circuitry is ***generally described*** in the '314 patent's specification. *See* Response Br., 30. However, nowhere in the disclosure of the '314 patent cited by Netlist, or anywhere else, is there ***any disclosure of any structure that performs the specific "circuitry" functionality required by the claims***. Stone Decl., ¶ 59. Indeed, Netlist's string citation falls far short of showing a clear link or association between a structure in the '314 patent's specification and the "circuitry" functionality at issue here.

X. CONCLUSION

For the reasons stated herein, the Court should adopt Defendants' proposed constructions for the disputed terms and phrases.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that on this 24th day of March 2021 the foregoing document was electronically filed with the Clerk of Court using the Court's CM/ECF system which will send notification of such filing to all counsel of record, including counsel of record for Plaintiff Netlist.

/s/ Michael R Rueckheim
Michael Rueckheim